42. (New) The circuit of claim 22 further including automated test equipment coupled externally to the circuit and an intermediate register coupled between the automated test equipment and the decompression.

43. (New) The circuit of claim 42, wherein the intermediate register receives compressed test patterns from the automated test equipment and provides the compressed test patterns to the decompressor.

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44. (New) The circuit of claim 30, wherein the compressed test pattern is received while the decompressor decompresses the test pattern.

45. (New) The circuit of claim 30, further including automated test equipment coupled externally to the circuit and an intermediate register positioned between the automated test equipment and the decompressor.

46. (New) The circuit of claim 32, further including automated test equipment coupled externally to the circuit and an intermediate register positioned between the automated test equipment and the linear finite state machine.

47. (New) The circuit of claim 32, wherein the bits of the compressed test pattern are received while the decompressed pattern of bits are produced.

REMARKS

Claims 1 through 38 remain in the application. New claims 39-47 have been added to the application. Reconsideration is respectfully requested.

All claims were rejected under 35 U.S.C. §102(e) based on U.S. Patent No. 5,991,898 to Rajski, the same inventor as the subject application.